REMARKS

The claims are claims 1, 4, 5, 9 to 11, 13, 16 and 17.

Claims 1, 4, 5, 10, 11, 13, 16 and 17 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Pitsianis et al. Pub. No. US 2003/0088601 Al and Adelman et al. U.S. Patent No. 5,666,300.

Claims 1 and 13 recite subject matter not made obvious by the combination of Pitsianis et al and Adelman et al. Claim 1 recites "combining the first product with the second product to form a combined product and rounding the combined product to form an intermediate result via an arithmetic circuit having a first input receiving said first product, a second input receiving said second product and a carry input to a mid-position receiving said rounding value to form the intermediate result." Claim 13 similarly recites "an arithmetic circuit having a plurality of inputs each connected to receive a corresponding one of the plurality of products from the plurality of multipliers and a mid-position carry input for mid-position rounding responsive to the rounding dot product instruction." This recitation of the mid-position carry input for rounding represents subject matter neither taught in nor made obvious by the references. The FINAL REJECTION states at page 2, line 23 to page 3, line 6 that Pitsianis et al discloses:

> "rounding (627) the combined product to form an intermediate result via an arithmetic circuit (627) having a first input receiving said first product, a second input receiving said second product and a carry input to a mid-position receiving said rounding value to form the intermediate result (Figure 2B with rounding architecture and col. 3 0049-0054 wherein the carry-input is a rounding factor according to conventional rounding architecture as ROUND, TRUNC, CEIL, or FLOOR and in Figure 3B the shifting/dividing is done prior rounding)"

The RESPONSE TO ARGUMENTS of the FINAL REJECTION at page 5, line 15 to page 6, line 3 states:

> "The examiner respectfully submits that Figure 2B discloses different rounding modes including truncating, ceiling, flooring, and rounding mode. An instant case of an inherent and well known technique in the art for ceiling mode is to add a factor called carrying factor or rounding factor (either 0 or 1) to the rounding number (e.g. 33.6 will be 34 wherein 1 carry factor will be added to 33 for round up) to correctly round toward positive number. In addition, the MPYCX instruction in Figure 2B is rounding upper 16-bit portion of 30-bit in line 3 of table. From all above, there must be a carry input or carrying factor of certain rounding modes added to the last bit of upper 16-bit portion of the 30-bit result number."

The Applicants do not dispute that Pitsianis et al discloses rounding. The Applicants urge that the manner of rounding recited in claims 1 and 13 is unobvious over the manner of rounding disclosed in Pitsianis et al. Both claims 1 and 13 require the rounding to take place during the arithmetic combining of the two products. The bits to be output are selected by a later shifting. The use of a mid-position carry input is useful in this rounding. The normal manner of rounding using an arithmetic operation is to provide a carry input into the least significant bit of the arithmetic logic unit. Since this invention will eventually discard the least significant bits of the arithmetic combination, using this prior art technique would result in additional processing for the carry ripple of the rounding input. Claim 1 recites "a carry input to a mid-position receiving said rounding value to form the intermediate result." Claim 13 similarly recites "a mid-position carry input for mid-position rounding responsive to the rounding dot product instruction." Such a mid-position carry input causes the carry input to change only those bits that will be retained after the shifting. While the OFFICE ACTION states that this is

disclosed in Pitsianis et al, in fact neither subtractor 623, adder 625 of Figure 6 nor adder 723, subtractor 725 of Figure 7 illustrate the "mid-position carry input" recited in claims 1 and 13. The cited test of paragraphs [0049] to [0054] disclose rounding modes without disclosing the recited "mid-position carry input." Pitsianis et al discloses at paragraph [0054]:

> "The selection of the bits and rounding occurs in selection and rounder circuit 627."

and at paragraph [0055]:

> "The results from adder 723 and subtractor 725 still need to be selected and rounded in selection and rounder circuit 727 and the final rounded results stored in the target register 729 in the CRF."

Pitsianis et al teaches that rounding takes place in a different method step (claim 1) or in different structure (claim 13) than recited in the claims. Further, Pitsianis et al fails to teach a mid-position carry input. Accordingly, claims 1 and 13 are not made obvious by the combination of Pitsianis et al and Adelman et al.

Claims 16 and 17 recite subject matter not made obvious by the combination of Pitsianis et al and Adelman et al. Claim 16 recites "the step of shifting further includes sign extending the intermediate result." Claim 17 recites the shifter "sign extends the output of the arithmetic circuit." The FINAL REJECTION cites rounder circuit 627 illustrated in Figure 6 of Pitsianis et al as disclosing this element in "selecting only 30-15 out of 32 bits." The FINAL REJECTION further states it would be obvious to substitute the shifter illustrated in Figure 2 of Adelman et al for the selector of Pitsianis et al. The RESPONSE TO ARGUMENTS of the FINAL REJECTION at page 6, lines 6 to 10 states:

> "The examiner respectfully submits that Figure 18 clearly shows a sign of operand must maintain throughout the operations in order to provide the correct result. In addition, the shifting and selecting process is selecting upper 16-bit portion including the most significant bit (MSB) as signed bit. Therefore, the cited reference of Pitsianis et al. inherently disclose an 'sign extending' in operations."

The Applicant respectfully submits this is in error. "Sign extending" and "sign extend" are terms known in the art. A signed number has a most significant bit indicating the sign. A "0" indicates a positive number while a "1" indicates a negative number. Sign extension duplicates this most significant bit to maintain the sign indication following the shift operation. Pitsianis et al include no such disclosure. In fact, Pitsianis et al includes no teaching of signed numbers and therefore cannot teach the claimed sign extension. The additional teaching of Pitsianis et al regarding Figure 18 concerns addition for some inputs to adders 1823 and 1825 and subtraction for other inputs. Adelman et al does disclose "sign extension" in conjunction with accumulator registers 83 and 84 where 8-bit registers A2 and B2 store a sign extension. Neither Pitsianis et al nor Adelman et al teach sign extension during shifting as recited in claim 1 or sign extension by a shifter as recited in claim 13. Accordingly, claims 16 and 17 are allowable over the combination of Pitsianis et al and Adelman et al.

Claims 4, 5 and 9 to 11 are allowable by dependence upon respective allowable base claims 1 and 13.

The Applicants respectfully request entry and consideration of this amendment. Entry of this amendment is proper at this time because the amendment serves only to clarify subject matter previously recited. Thus no new search or reconsideration is required.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early entry of this amendment, reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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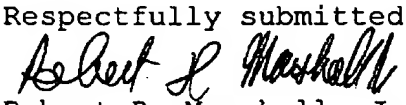
Respectfully submitted,



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